KENYATTA UNIVERSITY

UNIVERSITY EXAMINATIONS 2011/2012

SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONICS ENGINEERING

EEE 207: ANALOGUE ELECTRONICS I

DATE: THURSDAY 12TH APRIL 2012 **TIME: 2.00 P.M. – 4.00 P.M.**

INSTRUCTIONS

*Answer **Question 1** and any other **Two** questions*
Show all working in a neat and legible manner

QI

(a)

(i) Explain how the addition of an impurity in an intrinsic semiconductor material improves the conductivity of a semiconductor. (4 marks)

(ii) Explain the V1 characteristics of a PN junction diode. (2 marks)

(b)

(i) Explain the principle of operation of a Zener diode. (2 marks)

(ii) A motorola 1N 746 Zener diode is being operated at 75°C. Calculate the maximum power dissipation rating of the device. Assume that the d.c power dispation of the device is 500mW and the derating factor is 3.33mW/^{0}C above 50^{0}C. (2 marks)

(c)

(i) Explain the principle of operation of a transistor in an amplifier. (2 marks)

(ii) Explain some of the important points of comparison between field-effect transistor and bipolar junction transistor. (2 marks)

(d)

(i) Describe the different classes of power amplifier. (2 marks)

(ii) Explain the principle of operation of push-pul amplifier and discuss the advantages of class B push – pull amplifier. (5 marks)

(e)

(i) With the aid of a block diagram, explain how negative feedback is achieved. (2 marks)

(ii) An engineer designs an amplifier to have a voltage gain of 80, but when constructed it gives only a voltage gain of 60. A technician suggests that a positive feedback may be introduced to increase the gain to the required level. Determine the feedback which should be given to increase the voltage gain to the required level. (2 marks)

(f)

(i) Derive the expression for the lower cut-off frequency of a BJT amplifier. (3 marks)

(ii) For the network shown in Fg Q1(f) determine the break frequency, sketch the assmptotes, locate the -3dB point and sketch the frequency response curve. (4 marks)

Fig. Q1 (f)

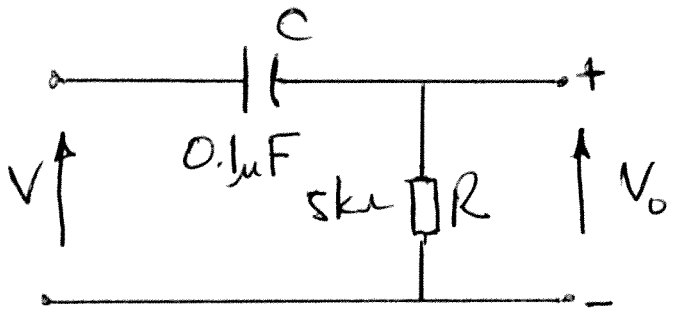
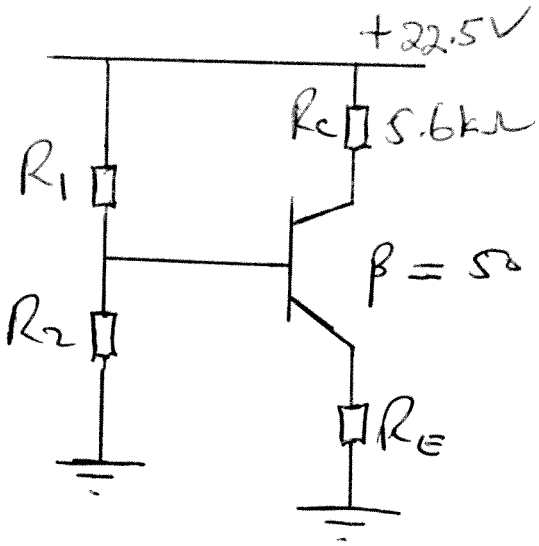


Fig. Q2 (b)



Q2

(a)

(i) Explain why it is necessary to bias the transistor in order to use it in any application. (4 marks)

(ii) Describe the different methods used for transistor biasing. (4 marks)

(b) A transistor with $\beta = 50$, $V_{BE} = 0.7V$, $V_{cc} = 22.5$ V and $Rc = 5.6k\Omega$ is used in a biasing circuit as shown in figQ2 (b). It is designed to establish the quiescent point at $V_{CE} = 12V$, $I_C = 1.5mA$ and stability factor $S \leq 3$. Determine the values of resistor R_E, R_1 and R_2. (12 marks)

Q3

(a)

(i) With the aid of a block diagram, derive the h-parameter model for a transistor. Explain how the voltage gain, current gain, input resistance and output resistance can be obtained using h-parameters. (12 marks)

(b) A common-emitter amplifier with voltage divider bias has values of $Rc = 12k\Omega$, $R_L = 4.7\ k\Omega$, $R_1 = 33k\Omega$ $R_2 = 4.7k\Omega$ and $I = 1mA$. The transistor has h-parameters values of hie $= 1k\Omega$ to $5k\Omega$ and hfe = 70 to 350. Determine the value of

(i) input impendence

(ii) overall gain for the circuit. (8 marks)

Q4

(a)

(i) Explain the condition which must be met for oscillations to occur in an amplifier. (4 marks)

(ii) Describe the different methods for connecting the feedback signed from the amplifier output to the input. (4 marks)

(b) The circuit components for a series-shunt pair type two stage amplifier using transistor with hfe = 99 and hie = $2k\Omega$ are as follows: Load resistance of first stage $Rc = 22k\Omega$ Emitter resistance of first stage $R_4 = 100\Omega$.
biasing resistors of second stage (R_1 and R_2) = 22 and $22k\Omega$ Load resistance of second Stage (R^1c) = $4.7k\Omega$ feedback resistor from collector of second stage to emitter of first Stage (R_3) = $7.8k\Omega$. Calculate the voltage gain, input resistance and output resistance of the amplifier. (12 marks)

Q5

(a)

(i) Explain the difference between the voltage amplifier and power amplifier. (4 marks)

(ii) Describe what is meant by d.c and a.c load lines in an amplifier. (6 marks)

(iii)Show that the maximum collector efficiency for a class A amplifier is 50%. (4 marks)

(b) A single –stage class A amplifier has $V_{cc} = 20V$, $V_{CEO} = 10V$, $Ic\varphi = 600mA$ and collector load resistor $R_L = 16\Omega$. The a.c output current varies by $\pm 300mA$ with the a.c input signal. Determine:

(i) Power supplied by the d.c source to the amplifier circuit.

(ii) D.C power consumed by the load resistor.

(iii)a.c power developed across the load resistor.

(iv)d.c power delivered to the transistor

(v) d.c power wasted in transistor collector.

(vi)Overall efficiency. (6 marks)