KENYATTA UNIVERSITY

UNIVERSITY EXAMINATIONS 2011/2012

SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER ENGINEERING

SCE 316: DIGITAL ELECTRONICS II

DATE: Friday, 13th April, 2012 TIME: 11.00 a.m. – 1.00 p.m.

(i) This paper contains **FIVE** questions.
(ii) Answer question **1** and any other **TWO** questions

Question 1(COMPULSORY)

a)

i) Explain the difference between an encoder and a decoder **(2 marks)**

ii) How does a priority encoder differ from an ordinary encoder? **(1mark)**

b) What is a multiplexer? **(2 marks)**

c)State THREE applications of multiplexers **(3 marks)**

d)Draw a block diagram symbol and the truth table for a 1-line-8-line demultiplexer **(4 marks)**

e)Give definitions of the following terms referred in DAC?

i) Accuracy **(2 marks)**
ii) Settling time **(2 marks)**
iii) Resolution **(2 marks)**

f) A Certain clocked R-S Flip Flop has set up and hold times specified typically as t_s = 30 ns and t_h = 5 ns

i) What is the minimum amount of time that the R and S inputs have to be HIGH before the CLK input transition occurs? **(1 mark)**

ii) How long must the R and S inputs remain in the HIGH state once the CLK transition occurs **(1 mark)**

Question 2:

a) Design a logic circuit for the **e** and **g** output of a BCD to 7 segment decoder with active LOW outputs showing the truth table and a simplified expression for each output **(10 marks)**

b) What is the advantage of an flash EPROM over a EEPROM? **(5 marks)**

c) Draw a block diagram of a 74150 data selector being used to solve the logic problem described by the Boolean expression ***A'B'C'D + A'BCD + ABCD' + AB'C'D' + ABCD = Y.*** **(5 marks)**

Question 3:

a) An analog voltage of the range of –V to +V is required to be converted into 3-bit 2's complement digital format. The digital value for 0 V should be 000 and the maximum quantization error should not exceed ± LSB. Determine the quantization interval **(5 marks)**

b) Design a D/A converter for 4-bit digital inputs in 1's complement format (5 **marks)**

c) Explain the fundamental difference between **A/D** and **D/A** converters. **(3 marks)**

d) When the output of a flip-flop goes LOW, HIGH, LOW, HIGH on repeated clock pulses, it is in what mode of operation? **(2marks)**

Question 4:

Suppose an input to a recognizer circuit is given as **11100110100100110**. The rcognizer circuit has only one input **X**. There is also one output **Z** which is a **1** when the desired pattern is realized/found. Using sequence recognizer to detect the pattern **1001**.

a) What will be the output if one bit of input is supplied on every clock cycle **(5 marks)**

b) Design a JK flip flop based circuit with the state diagram shown in the Figure 4.1, show all your working including the final circuit diagram **(15 marks)**

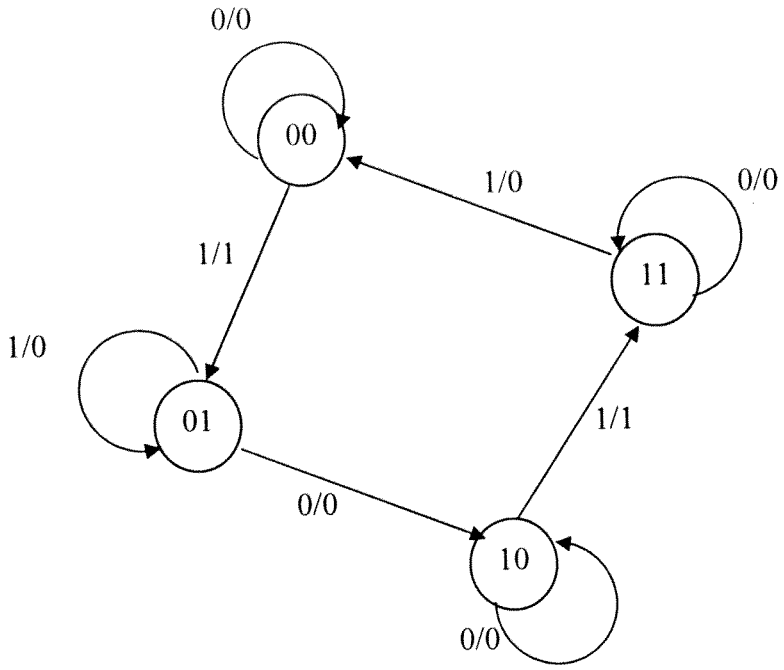

Figure4.1

Question 5:

Design a BCD to decimal decorder with the use of an active HIGH decoder. In your design show,

a) The truth table **(5 marks)**

b) Simplified expression for the outputs D0, D1 and D3 **(5 marks)**

c) What will be the expression for D0,D1, and D3 if you use an active LOW decoder? **(5 marks)**

d) There are two types of seven segment decoder displays i.e the Common Cathode and Common Anodes. Distinguish between the two? **(5 marks)**