KENYATTA UNIVERSITY

UNIVERSITY EXAMINATIONS 2011/2012

SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE (COMPUTER ENGINEERING)

SCE 515: PROGRAMMABLE DEVICES

DATE: Friday, 13th April, 2012 TIME: 2.00 p.m. – 4.00 p.m.

INSTRUCTIONS:

Answer three questions. Question ONE is compulsory. Each question has equal marks.

Q1.

(a) Discuss the key advantages of Programmable Logic Device over logical discrete circuitry (2Marks)

(b) Enumerate the different types of PLD and give a short description of each (2 marks)

(c) Write a function that implements the cube of numbers on a 32 bit ROM device using a 3 bit input multiplexer and 8 bit data output. (4 marks)

(d) Discuss the importance of circuit optimization for PLD, and identify three methods used to calculate the cost and two methods used to minimize circuits cost and size (4 marks)

(e) Describe the following HDL concepts

i. Behaviour Modelling (1 marks)
ii. Structural Modelling (1 marks)
iii. RTL (1 mark)
iv. Syntheses (1 marks)

(f) Distinguish between Program I/O and interrupt driven I/O (2marks)

(g) Identify three design characteristics that differentiate a microprocessor from a microcontroller (2 marks)

KENYATTA UNIVERSITY
UNIVERSITY EXAMINATIONS 2011/2012
SECOND SEMESTER EXAMINATIONS FOR DEGREE OF
BACHELOR OF SCIENCE (COMPUTER ENGINEERING)
SCE 512 PROGRAMABLE DEVICES

Q2.

(a) Three methods used to calculate the cost and two methods used to minimize circuits cost and size (2 marks)

(b) Calculate the Literal cost(L), gate input cost (G) and gate input with NOT (GN) for the following functions represented by the following gate circuits. (4 marks)

i. $F = BD + A\overline{B}C + A\,\overline{C}\,\overline{D}$
ii. $F = BD + A\overline{B}C + A\,\overline{B}\,\overline{D} + AB\overline{C}$
iii. $F = (A + B)(A + D)(B + C + D)(\overline{B} + \overline{C} + \overline{D})$

(c) Using K-Map minimization technique, derive a SOP for the following (6 marks)

$$\sum_{W,X,Y,Z}(3,4,5,7.9,13,14,15)$$

(d) The following functions are required for developing a combinational circuit.

$W = AB\overline{C} + \overline{A}\,\overline{B}\,C\,\overline{D}$

$X = A + BCD$

$Y = \overline{A}B + CD + \overline{B}\,\overline{D}$

$Z = A\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C + AB\,\overline{C} + \overline{A}\,\overline{B}\,C\,\overline{D}$

Develop the following

i. Identify sharable terms (2 marks)
ii. Truth table to program a PAL circuit device (3 marks)

Program the PAL circuit using the derived truth table on schematic diagram provided. (3marks).

KENYATTA UNIVERSITY
UNIVERSITY EXAMINATIONS 2011/2012
SECOND SEMESTER EXAMINATIONS FOR DEGREE OF
BACHELOR OF SCIENCE (COMPUTER ENGINEERING)
SCE 512 PROGRAMABLE DEVICES

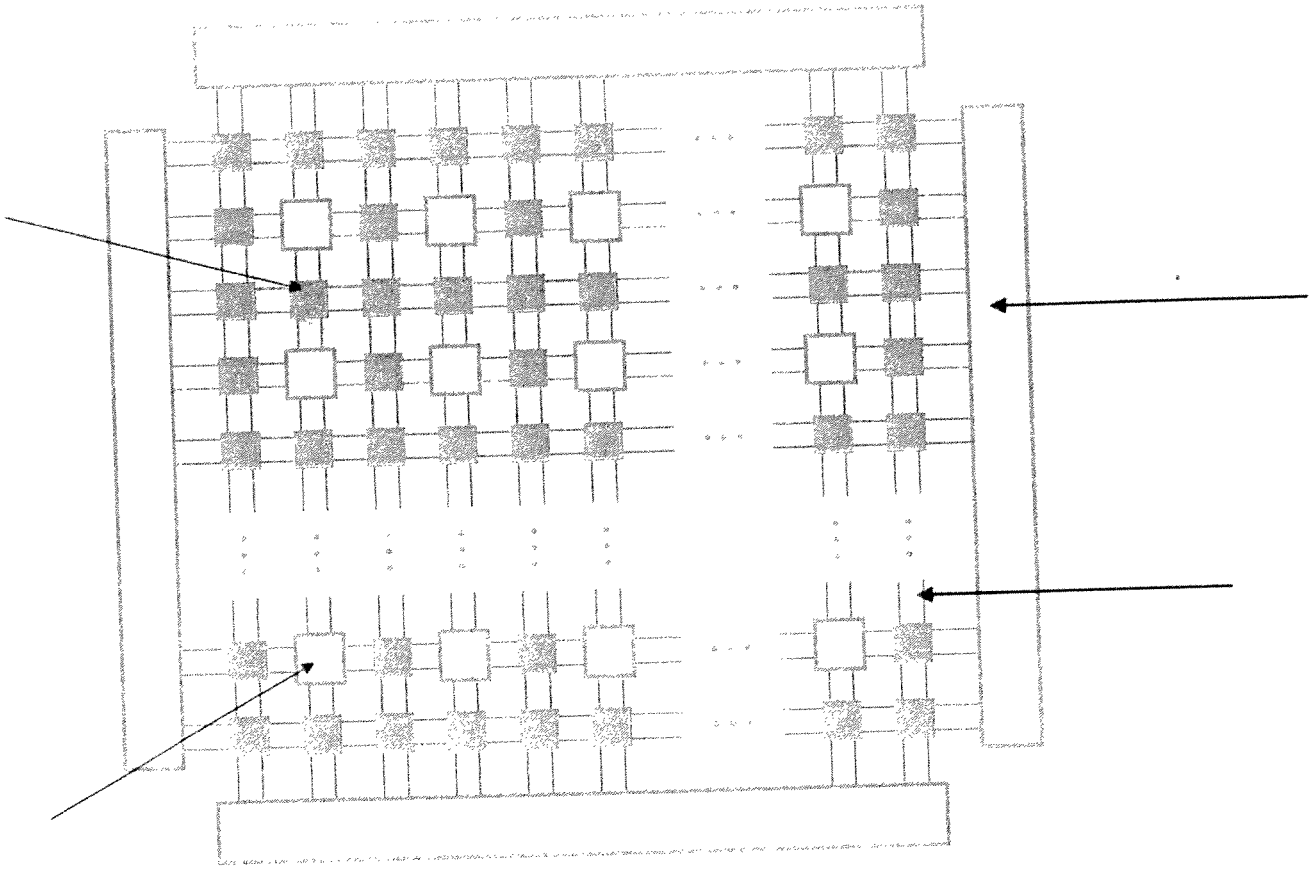
Q3.

(a) Identify the factors that have seen the preference of FPGA as the choice PLD (2 marks)

(b) Use a diagram to differentiate between a combinational circuit and a sequential circuit (4 marks)

(c) Discuss why In System Programming (ISP) and Joint Test Action Group (JTAG) are preferred for programming PLDs (4)

(d) Discuss purpose of the various structure of a FPGA and describe the various methods used to burn logic and how this differs from other PLD's such as ROM and CPLD (6 marks)



KENYATTA UNIVERSITY
UNIVERSITY EXAMINATIONS 2011/2012
SECOND SEMESTER EXAMINATIONS FOR DEGREE OF
BACHELOR OF SCIENCE (COMPUTER ENGINEERING)
SCE 512 PROGRAMABLE DEVICES

Q4

(a) Discuss the advantage of HDL/IP circuits in the design of circuits using PLD (2 marks).

(b) Using a flow diagram show the process required to design a circuit using CAD system and HDL for FPGA's (4 marks).

(c) The HDL below is written in Verilog and represents an adder.

module FA (input [3:0],a,b, cin, output [3:0] cout, sum)

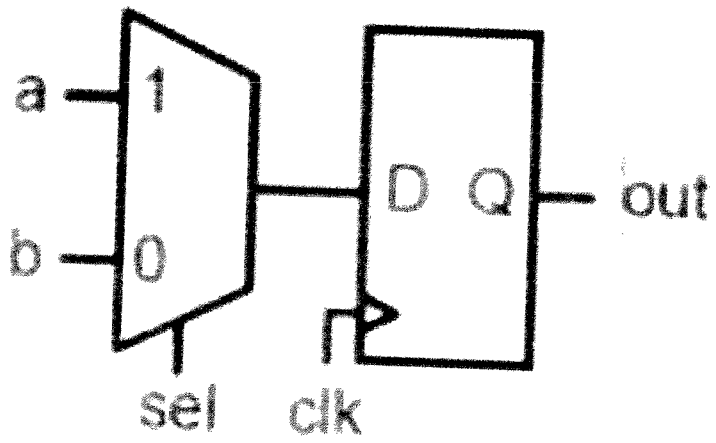
// adding logic

end module;

(i) Draw a schematic diagram showing the inputs and outputs of the circuit. (4 marks)

(ii) Using Verilog script show how two of the above modules can be combined together to increase the size of the input and output (6 marks)

(d) Write a Verilog Script for a positive edge 2:1 clocked multiplexer shown below. (4marks)



KENYATTA UNIVERSITY
UNIVERSITY EXAMINATIONS 2011/2012
SECOND SEMESTER EXAMINATIONS FOR DEGREE OF
BACHELOR OF SCIENCE (COMPUTER ENGINEERING)
SCE 512 PROGRAMABLE DEVICES

Q3

(a) Discuss the advantages/disadvantages of using Microcontrollers as programmable device.(4 marks)

(b) Explain how the 8051 microprocessor differentiates I/O and memory. (4 marks)

(c) With the aid of a block diagram illustration list the basic features of 8051 microcontroller (6 marks)

(d) The following code is written for a 8051 processor explain what each of the steps do and the general result of the code (6 marks)

```
org         0000h
loop:
            mov     b, #0FFh
            acall   delay
            clr     p1.0
            mov     b, #0FFh
            acall   delay
            mov     p1, #0FFh
            ajmp    loop

delay:
            djnz    acc, delay
            mov     acc, #0FFh
            djnz    b, delay
            ret
end
```

KENYATTA UNIVERSITY

UNIVERSITY EXAMINATIONS 2011/2012

SECOND SEMESTER EXAMINATIONS FOR DEGREE OF BACHELOR OF SCIENCE (COMPUTER ENGINEERING)

SCE 512 PROGRAMABLE DEVICES