KENYATTA UNIVERSITY

UNIVERSITY EXAMINATIONS 2011/2012

SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER TECHNOLOGY

SCT 106: DIGITAL SYSTEMS I

DATE: THURSDAY 12TH APRIL 2012 **TIME: 2.00 P.M. – 4.00 P.M.**

INSTRUCTIONS

- Students from Computing and Information Technology to attempt questions in Section I.
- Students from Electronic and Electrical Engineering department to attempt questions in Section II

SECTION I *(COMPUTER SCIENCE STUDENTS)*

Attempt question One and any other Two Questions from the same questions

QUESTION ONE

(a) Describe with the help of suitable diagrams the difference between a digital and an analogue signal. (4 marks)

(b) Perform the following conversions

(i) 24_{10} to binary

(ii) 1101.11_2 to decimal

(iii) AB_{16} to decimal

(iv) 250_{10} to hexa-decimal (8 marks)

(c) (i) State De-Morgan's Theorems (2 marks)

(ii) Simplify using Boolean algebra, the following logic expression

$$F = \overline{(A+B)\bar{C} + \bar{A}(B+C)}$$ (5 marks)

(i) Distinguish between combinational and sequential logic circuit.

(ii) What is a multiplexer? Describe with the help of suitable logic circuit, the operation of a 2 to 1 multiplexer. (11 marks)

QUESTION TWO

(a) Describe any TWO merits of digital circuits. (4 marks)

(b) What is a flip-flop? Briefly describe the operation of an R-S flip-flop. (6 marks)

(c) Using Karnaugh mapping, simplify the following logic expressions:

(i) $F = ABC + \bar{A}BC + A\bar{C} + B$

(ii) $F = \bar{A} + BC + A\bar{B}\bar{C} + A\bar{B}C + B\bar{C} + \bar{A}B$ (10 marks)

QUESTION THREE

(a) Describe the following terms

(i) Synchronous counters

(ii) Modulo of counter

(iii) Down counter (3 marks)

(b) Using three falling edge triggered JK flip flops, draw logic circuit of a 3-bit Asynchronous Up-counter and sketch timing diagrams at respective output Q_A, Q_B and Q_C for up to 8 pulses given that output from Q_A is the least significant bit while that from Q_C is the most significant. (13 marks)

(c) State ONE advantage and disadvantage of

(i) Synchronous counter

(ii) Asynchronous counter (4 marks)

QUESTION FOUR

(a) What is a de-multiplexer? With the help of a suitable logic circuit describe the operation of 1 to 2 de-multiplexer. (8 marks)

b) Illustrate how an OR gate can be implemented using NAND gates only. (4 marks)

(b) Determine the logic functions expressed by the following shorthand forms:

(i) $f(ABC) = \sum 0,2,3,5$ (simplify the determined expression)

(ii) $f(A,B,C) = \prod 1,3,4$ (simplification not required) (8 marks)

QUESTION FIVE

(a) Differentiate between an encoder and a decoder. (2 marks)

(b) Describe a Half-Adder and with the help of a suitable truth table, implement its logic circuit. (8 makrs)

c) (i) Determine the Excess-3 code for the decimal number 597. (5 marks)

(ii) Perform the following subtraction using 2's complement: 7_{10}-5_{10}. (5 marks)

SECTION II (*SOFTWARE ENGINEERING*)

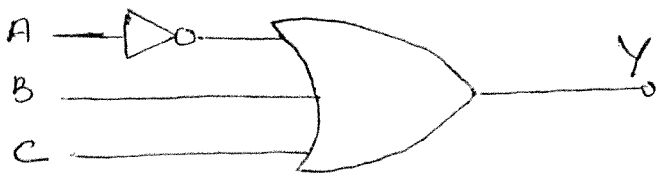
Attempt question One and any other Two questions from the same section

Question 1 (30 marks)

(a) Using NOR gates ONLY implement 2-input AND gate logic function and draw the circuit. (4 marks)

(b) Convert the binary number 101101.101_2 to its equivalent decimal number. (4 marks)

(c) Obtain the truth table for the logic circuit below. (4 marks)



(d) Using diagram(s) where possible discuss ANY TWO applications of flip flogs. (4 marks)

(e) Using J-K flip flop, design a circuit for 3 stage negative edge triggered flip flop and draw the timing diagram. (4 marks)

(f) Implement half-adder logic circuit and draw the truth table. (5 marks)

(g) Minimise the logic expression $F(A,B,C) = \Sigma(0,1,4,6,9)$ using Karnaugh map technique and draw the resulting circuit after minimization. (5 marks)

Question 2 (20 marks)

(a) Perform conversion of the following

(i) 51 (decimal) to binary

(ii) 37 (octal) to decimal

(iii) 8A (hexadecimal) to decimal (5 marks)

(b) Design a logic circuit having three inputs A, B, C such that output Y is 1 when A = 0 or whenever B = C = 1, then implement the circuit using NAND gates only. (5 marks)

(c) Design a 4-bit presettable counter and explain its operation. (5 marks)

(d) Draw a logic circuit to implement the function F = AB + A(B + C) + B (B + C). Simply the function using boolean algebra and draw logic circuit for simplified function. (5 marks)

Question 3 (20 marks)

(a) Perform the following operations

(i) Addition of 365 and 415 in octal

(ii) Addition of 945, 631 and 769 in BCD (5 marks)

(b) Implement the logic circuit for 4 input to one multiplexer and explain the operation. (5 marks)

(c) Design a parallel in–serial out 4-bit shift register and explain how 1011 input is shifted through the register. (5 marks)

(d) Simply the following expression using K-map and draw the resulting circuit. (5 marks)

$F(A,B,C,D) = \sum(0,3,6,7,9,13,14,15)$.

Question 4 (20 marks)

(a) If A = -24 and B = +16

(i) represent A and B in 8-bit 2's complement

(ii) find A + B (5 marks)

(b) Using circuit diagram explain the operation of a clocked RS flip flop and draw the truth table. (5 marks)

(c) Implement the boolean function $F = AB + \overline{A}C$ using NAND gates only and draw the circuit. (5 marks)

(d) Using a diagram explain the operation of a master-slave JK flip flop. (5 marks)

Question 5 (20 marks)

(a) Differentiate the following:

(i) Combinational and sequential logic

(ii) Synchronous and Asynchronous data transfer. (5 marks)

(b) Perform the following addition

(i) Binary 110110
110100
100111

(ii) Hexadecimal
F F E A
3 4 6 9
5 6 9 9 (5 marks)

(c) Explain the operation of a four bit binary decoder. (5 marks)

(d) Obtain the truth table/function table for the Boolean expression

$F = AB + \overline{C}A + C$ (5 marks)

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