KENYATTA UNIVERSITY

INSTITUTE OF OPEN LEARNING

UNIVERSITY EXAMINATIONS 2008/2009

EXAMINATION FOR THE DEGREE OF INFORMATION TECHNOLOGY

SIT 311: COMPUTER ARCHITECTURE

DATE: TUESDAY 13TH JANUARY 2009 TIME: 8.00 A.M. – 10.00 A.M.

INSTRUCTIONS:

- **Attempt question ONE and any other TWO questions.**

QUESTION 1

a) (i) Compute –3 - 4 in 4-bit complement notation.

(ii) A digital system has

V_{DD} 3.3 v, V_{IH} =1.2 v, V_{OL} = 0.7v, V_{IH} = 2.1v, V_{OH} =3.0v.

Calculate the noise margin of this signaling convention.

b) Using 8-bit two's complement integers, perform the following computation

(i) – 34 + (- 12)

(ii) 18 – (- 5)

c) (i) Explain why it is necessary for a computer system to provide a privileged mode and a user mode for programs

(ii) Describe the difference between RAM and ROM.

d) (i) State two advantages of stack-bases architecture over GPR architecture.

(ii) Briefly explain how instructions in a GPR architecture access their operands.

e) Explain the limits on how much a processor can be improved using pipelining.

QUESTION 2

a) Determine the binary and hexadecimal representations of the decimal number 47.

b) Using single-precision floating numbers, multiply 2.5 by 0.75.

QUESTION 3

a) Explain why self-modifying programmes are less common today than they were on early computers.

b) Describe the trade-offs involved whe using a single I/O bus for all of the devices connected to a given system

QUESTION 4

a) Briefly explain the difference between two-operand and three-operand instructions formats.

c) If a processor operates on 8-bit data types and a processor multimedia vector instructions operate on 64-bit data words, determine the maximum speedup that can be achieved by using multimedia vector instruction. Assume that all instructions take the same amount of time to execute

QUESTION 5

a) Explain why pipelining improves performance.

b) Describe why maintaining inclusion between different levels of the memory hierarchy makes implementing write-back memory hierarchy easier.

c) A cache has a capacity of 16 KB and a line length of 128 bytes. Calculate the number of sets the cache has if it is a 2-way, 4-way or 8-way set-associative.

==========